

DATA SHEET

74F841/842 Bus interface latches

Product data
Replaces datasheet 74F841/842/843/845/846 of 1999 Jun 23

2004 Jan 23

10-bit bus interface latches, non-inverting/inverting (3-State)

74F841/74F842

FEATURES

- High speed parallel latches
- Extra data width for wide address/data paths or buses carrying parity
- High impedance NPN base input structure minimizes bus loading
- I_{IL} is 20 μ A for minimum bus loading
- Buffered control inputs to reduce AC effects
- Ideal where high speed, light loading, or increased fan-in are required as with MOS microprocessors
- Positive and negative over-shoots are clamped to ground
- 3-State outputs glitch free during power-up and power-down
- 48 mA sink current
- Slim dual in-line 300 mil package
- Broadside pinout

DESCRIPTION

The 74F841 and 74F842 bus interface latches are designed to provide extra data width for wider address/data paths of buses carrying parity.

The 74F841 consists of ten D-type latches with 3-State outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. This allows asynchronous operation, as the output transition follows the data in transition. On the LE HIGH-to-LOW transition, the data that meets the set-up and hold time is latched.

Data appears on the bus when the Output Enable (\overline{OE}) is LOW. When \overline{OE} is HIGH the output is in the high-impedance state.

The 74F842 is the inverted output version of the 74F841.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F841, 74F842	5.5 ns	60 mA

ORDERING INFORMATION

COMMERCIAL RANGE: $V_{CC} = 5\text{ V} \pm 10\%$; $T_{amb} = 0^\circ\text{C to } +70^\circ\text{C}$

Type number	Package		
	Name	Description	Version
N74F841N, N74F842N	DIP24	plastic dual in-line package; 24 leads (300 mil)	SOT222-1
N74F841D, N74F842D	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

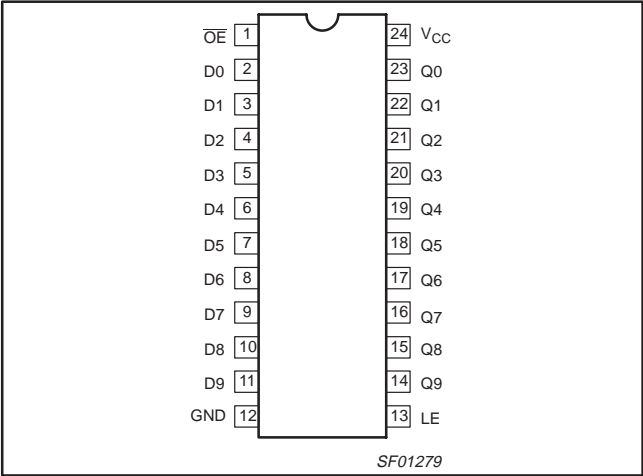
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Dn	Data inputs	1.0/0.033	20 μ A / 20 μ A
LE	Latch Enable input	1.0/0.033	20 μ A / 20 μ A
\overline{OE}	Output Enable input (active-LOW)	1.0/0.033	20 μ A / 20 μ A
Qn	Data outputs	1200/80	24 mA / 48 mA
\overline{Qn}	Data outputs	1200/80	24 mA / 48 mA

NOTE: One (1.0) FAST Unit Load is defined as: 20 μ A in the HIGH state and 0.6 mA in the LOW state.

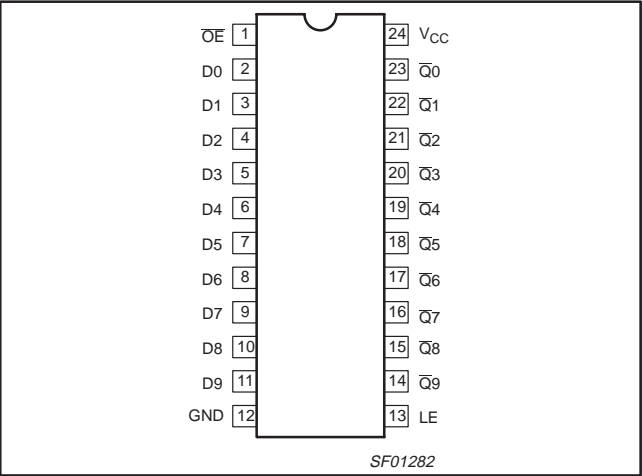
10-bit bus interface latches, non-inverting/inverting
(3-State)

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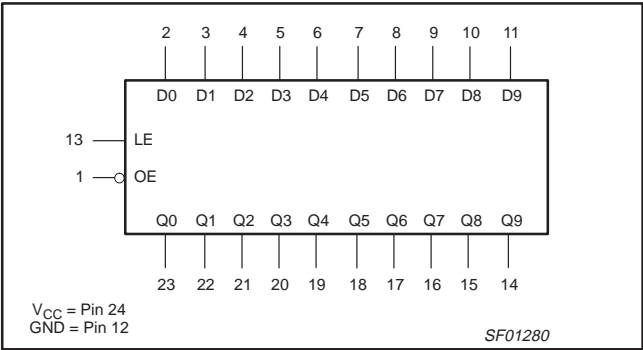
PIN CONFIGURATION for 74F841



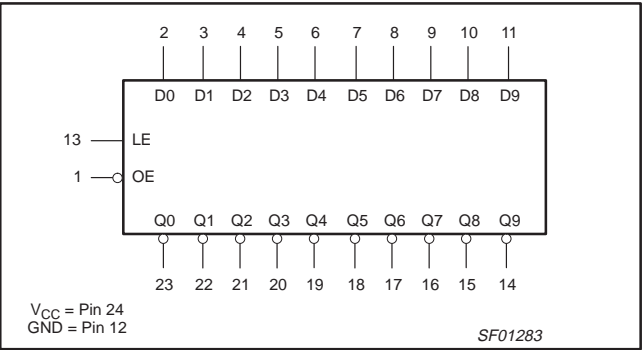
PIN CONFIGURATION for 74F842



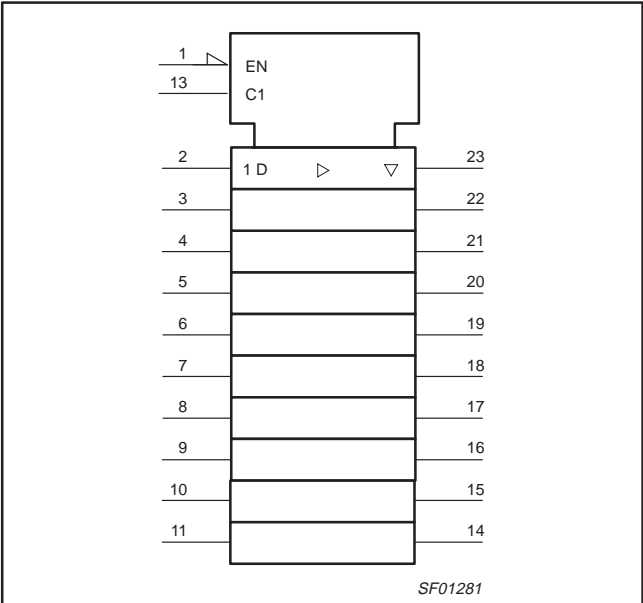
LOGIC SYMBOL for 74F841



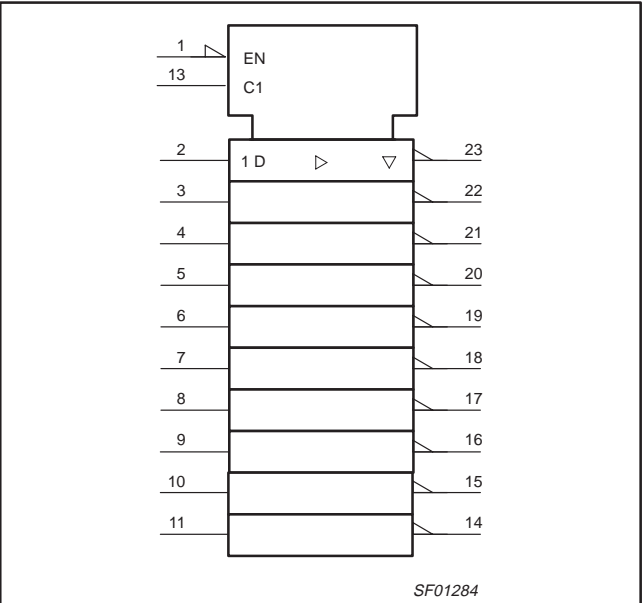
LOGIC SYMBOL for 74F842



LOGIC SYMBOL (IEEE/IEC) for 74F841



LOGIC SYMBOL (IEEE/IEC) for 74F842

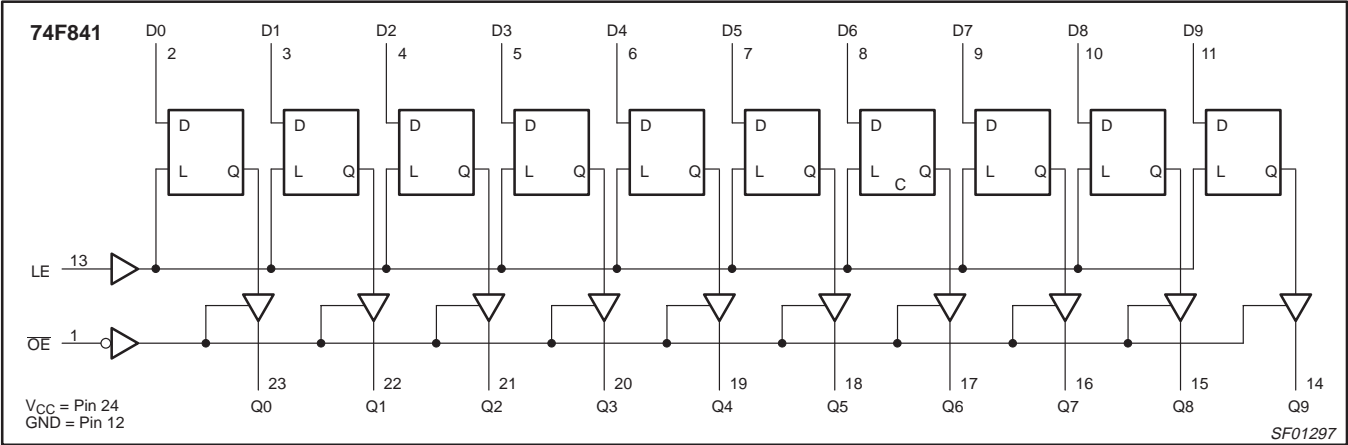


10-bit bus interface latches, non-inverting/inverting

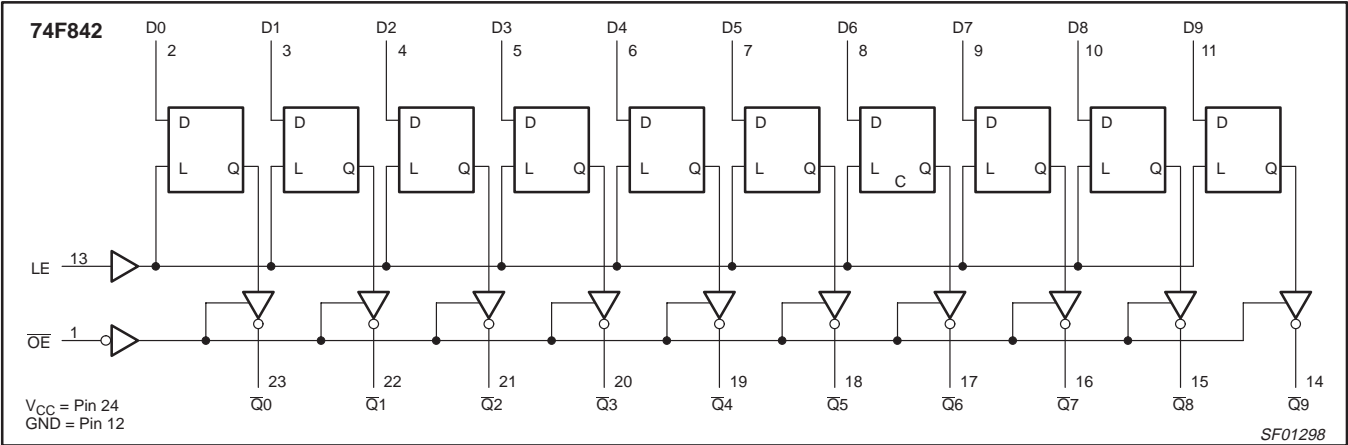
(3-State)

74F841/74F842

LOGIC DIAGRAM for 74F841



LOGIC DIAGRAM for 74F842



FUNCTION TABLE for 74F841 and 74F842

INPUTS			OUTPUTS		OPERATING MODE
			74F841	74F842	
\overline{OE}	LE	Dn	Qn	\overline{Qn}	
L	H	L	L	H	Transparent
L	H	H	H	L	
L	↓	l	L	H	Latched
L	↓	h	H	L	
H	X	X	Z	Z	High Impedance
L	L	X	NC	NC	Hold

H = HIGH voltage level
L = LOW voltage level
h = HIGH state one set-up time before the HIGH-to-LOW LE transition
l = LOW state one set-up time before the HIGH-to-LOW LE transition
↓ = HIGH-to-LOW transition
X = Don't care
NC = No change
Z = High impedance "off" state

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ABSOLUTE MAXIMUM RATINGS

Operation beyond the limits set forth in this table may impair the useful life of the device.

Unless otherwise noted these limits are over the operating free-air temperature range.

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	supply voltage	−0.5 to +7.0	V
V_{IN}	input voltage	−0.5 to +7.0	V
I_{IN}	input current	−30 to +5	mA
V_{OUT}	voltage applied to output in HIGH output state	−0.5 to V_{CC}	V
I_{OUT}	current applied to output in LOW output state	84	mA
T_{amb}	operating free-air temperature range	0 to +70	°C
T_{stg}	storage temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0	—	—	V
V_{IL}	LOW-level input voltage	—	—	0.8	V
I_{IK}	input clamp current	—	—	−18	mA
I_{OH}	HIGH-level output current	—	—	−24	mA
I_{OL}	LOW-level output current	—	—	48	mA
T_{amb}	operating free-air temperature range	0	—	+70	°C

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DC ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range unless otherwise noted.

SYMBOL	PARAMETER			TEST CONDITIONS ¹			LIMITS			UNIT
							MIN	TYP ²	MAX	
V _{OH}	HIGH-level output voltage			V _{CC} = MIN; V _{IL} = MAX; V _{IH} = MIN	I _{OH} = −15 mA	± 10%V _{CC}	2.2	–	–	V
						± 5%V _{CC}	2.2	3.3	–	V
				I _{OH} = −24 mA	± 10%V _{CC}	2.0	–	–	V	
					± 5%V _{CC}	2.0	–	–	V	
V _{OL}	LOW-level output voltage			V _{CC} = MIN; V _{IL} = MAX; V _{IH} = MIN	I _{OL} = 32 mA	± 10%V _{CC}	–	0.38	0.55	V
					I _{OL} = 48 mA	± 5%V _{CC}	–	0.38	0.55	V
V _{IK}	Input clamp voltage			V _{CC} = MIN; I _I = I _{IK}			–	−0.73	−1.2	V
I _I	Input current at maximum input voltage			V _{CC} = 0 V; V _I = 7.0 V			–	–	100	μA
I _{IH}	HIGH-level input current			V _{CC} = MAX; V _I = 2.7 V			–	–	20	μA
I _{IL}	LOW-level input current			V _{CC} = MAX; V _I = 0.5 V			–	–	−20	μA
I _{OZH}	Off-state output current, HIGH-level voltage applied			V _{CC} = MAX; V _O = 2.7 V			–	–	50	μA
I _{OZL}	Off-state output current, LOW-level voltage applied			V _{CC} = MAX; V _O = 0.5 V			–	–	−50	μA
I _{OS}	Short-circuit output current ³			V _{CC} = MAX			−100	–	−225	mA
I _{CC}	Supply current (total)	74F841	I _{CC} H	V _{CC} = MAX			–	50	65	mA
			I _{CC} L				–	60	80	mA
			I _{CC} Z				–	70	92	mA
		74F842	I _{CC} H	V _{CC} = MAX			–	40	60	mA
			I _{CC} L				–	65	90	mA
			I _{CC} Z				–	60	90	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5 V, T_{amb} = 25 °C.
- Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

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AC ELECTRICAL CHARACTERISTICS for 74F841/74F842

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T _{amb} = +25 °C V _{CC} = +5.0 V C _L = 50 pF; R _L = 500 Ω			T _{amb} = 0 °C to +70 °C V _{CC} = +5.0 V ± 10% C _L = 50 pF; R _L = 500 Ω		
				MIN	TYP	MAX	MIN	MAX	
t _{PLH} t _{PHL}	Propagation delay Dn to Qn	74F841	Waveform 1, 2	2.0 2.5	4.0 4.5	7.5 7.5	2.0 2.5	8.0 8.0	ns
t _{PLH} t _{PHL}	Propagation delay LE to Qn		Waveform 1, 2	4.5 4.0	6.5 6.0	9.5 9.0	4.0 3.5	10.0 9.5	ns
t _{PLH} t _{PHL}	Propagation delay Dn to Q̄n	74F842	Waveform 1, 2	3.5 3.0	5.5 5.0	8.5 8.0	4.5 4.0	9.0 8.5	ns
t _{PLH} t _{PHL}	Propagation delay LE to Q̄n		Waveform 1, 2	5.0 4.5	7.0 6.5	10.0 9.0	3.0 3.0	10.5 9.5	ns
t _{PZH} t _{PZL}	Output enable time HIGH or LOW-level OE to Qn or Q̄n		Waveform 4 Waveform 5	2.5 4.0	4.5 6.0	8.0 9.5	2.0 3.0	8.5 10.5	ns
t _{PHZ} t _{PLZ}	Output disable time HIGH or LOW-level OE to Qn or Q̄n		Waveform 4 Waveform 5	1.0 1.0	4.5 5.0	8.0 8.0	1.0 1.0	8.5 8.5	ns

AC SET-UP REQUIREMENTS for 74F841/74F842

SYMBOL	PARAMETER		TEST CONDITION	LIMITS				UNIT
				$T_{amb} = +25\text{ }^{\circ}\text{C}$ $V_{CC} = +5.0\text{ V}$ $C_L = 50\text{ pF}; R_L = 500\text{ }\Omega$		$T_{amb} = 0\text{ }^{\circ}\text{C to } +70\text{ }^{\circ}\text{C}$ $V_{CC} = +5.0\text{ V} \pm 10\%$ $C_L = 50\text{ pF}; R_L = 500\text{ }\Omega$		
				MIN	TYP	MIN	MAX	
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW Dn to LE		Waveform 3	0.0 0.0	— —	1.0 1.0	— —	ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW Dn to LE	74F841	Waveform 3	2.5 3.0	— —	3.0 4.0	— —	ns
$t_w(H)$	LE pulse width, HIGH		Waveform 3	3.5	—	4.0	—	ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW Dn to LE	74F842	Waveform 3	3.0 3.5	— —	3.5 4.5	— —	ns
$t_w(H)$	LE pulse width, HIGH		Waveform 3	3.0	—	3.0	—	ns

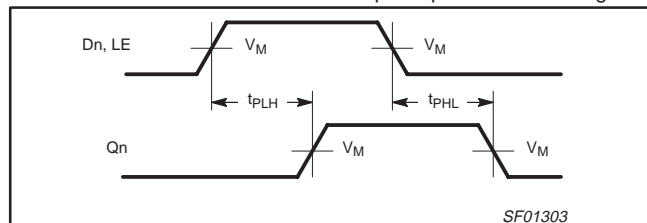
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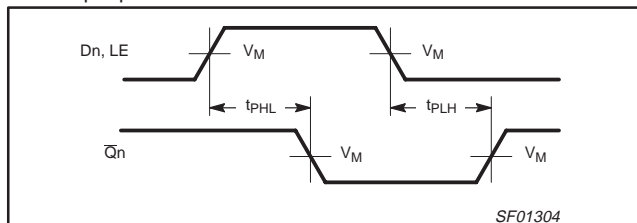
AC WAVEFORMS

For all waveforms, $V_M = 1.5$ V.

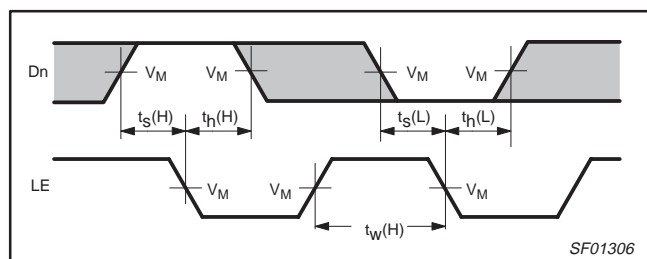
The shaded areas indicate when the input is permitted to change for predictable output performance.



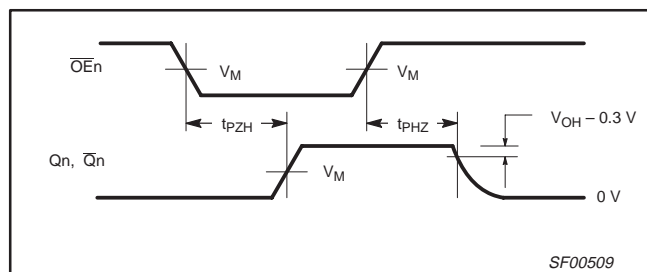
Waveform 1. Propagation delay, non-inverting path



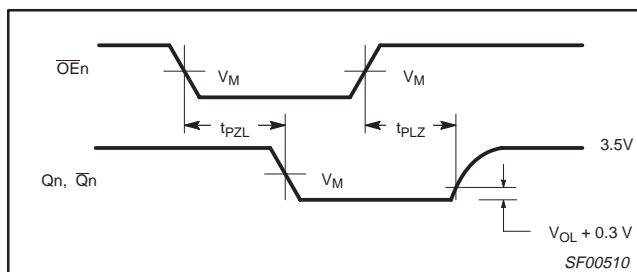
Waveform 2. Propagation delay, inverting path



Waveform 3. Data set-up and hold times



Waveform 4. 3-State Output Enable time to HIGH level and Output Disable time from HIGH level

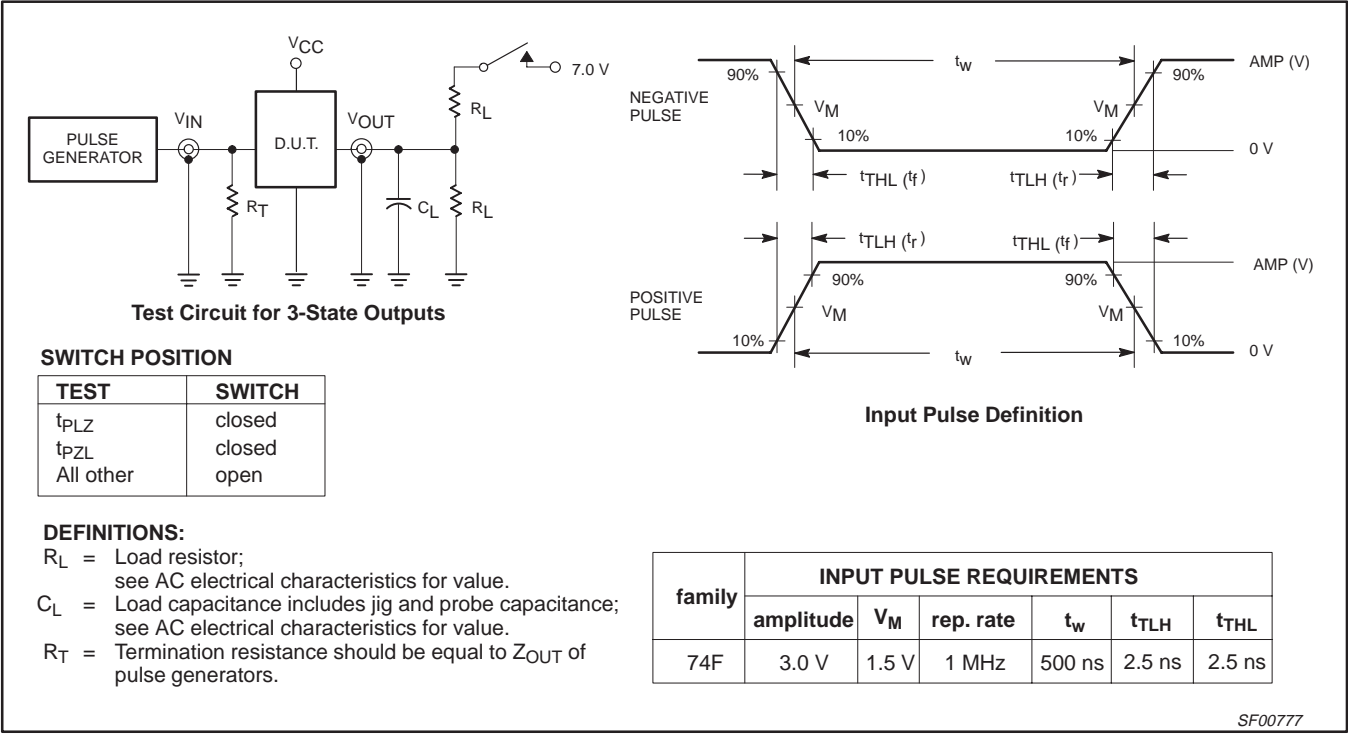


Waveform 5. 3-State Output Enable time to LOW level and Output Disable time from LOW level

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TEST CIRCUIT AND WAVEFORMS

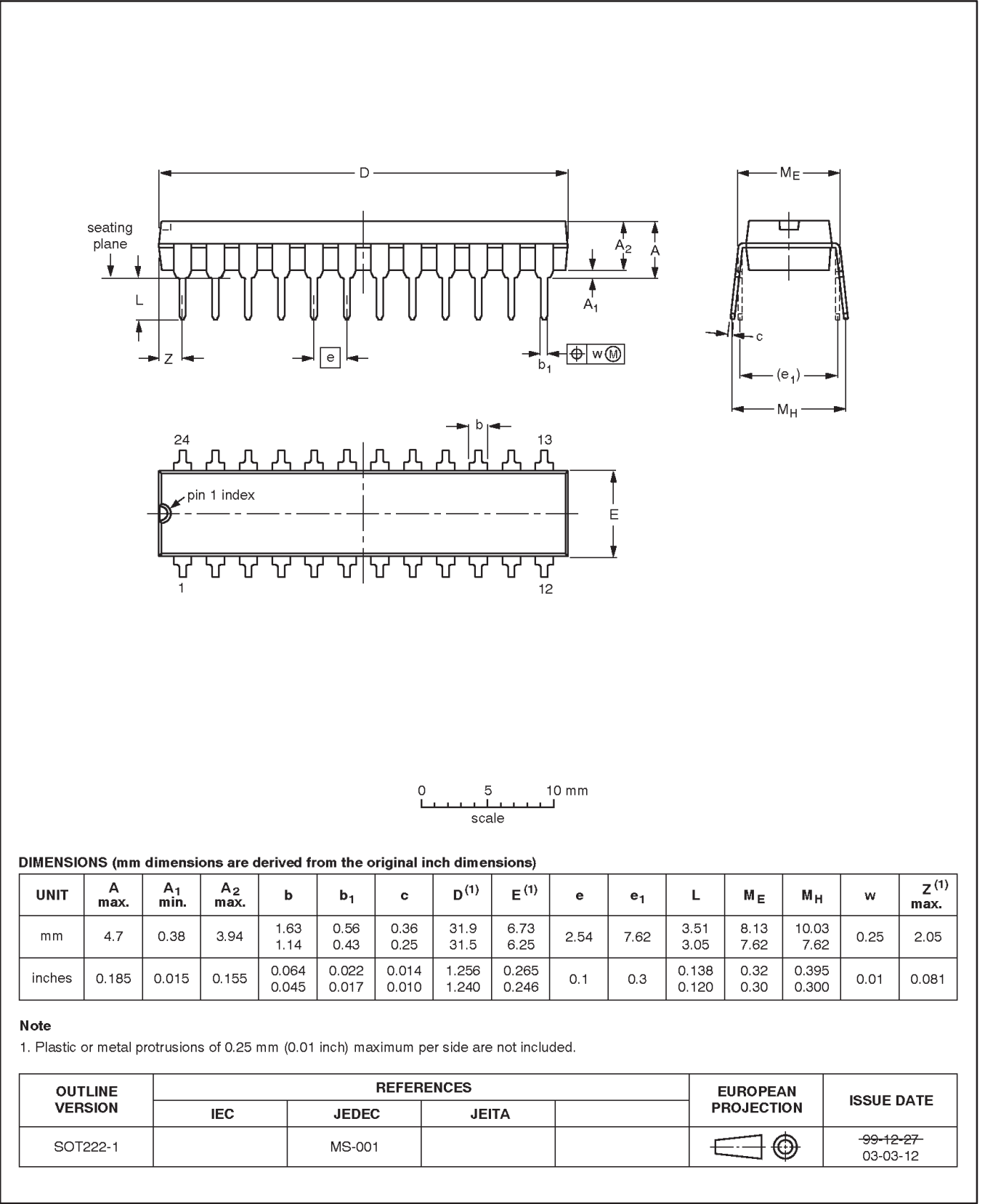


10-bit bus interface latches, non-inverting/inverting
(3-State)

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DIP24: plastic dual in-line package; 24 leads (300 mil)

SOT222-1

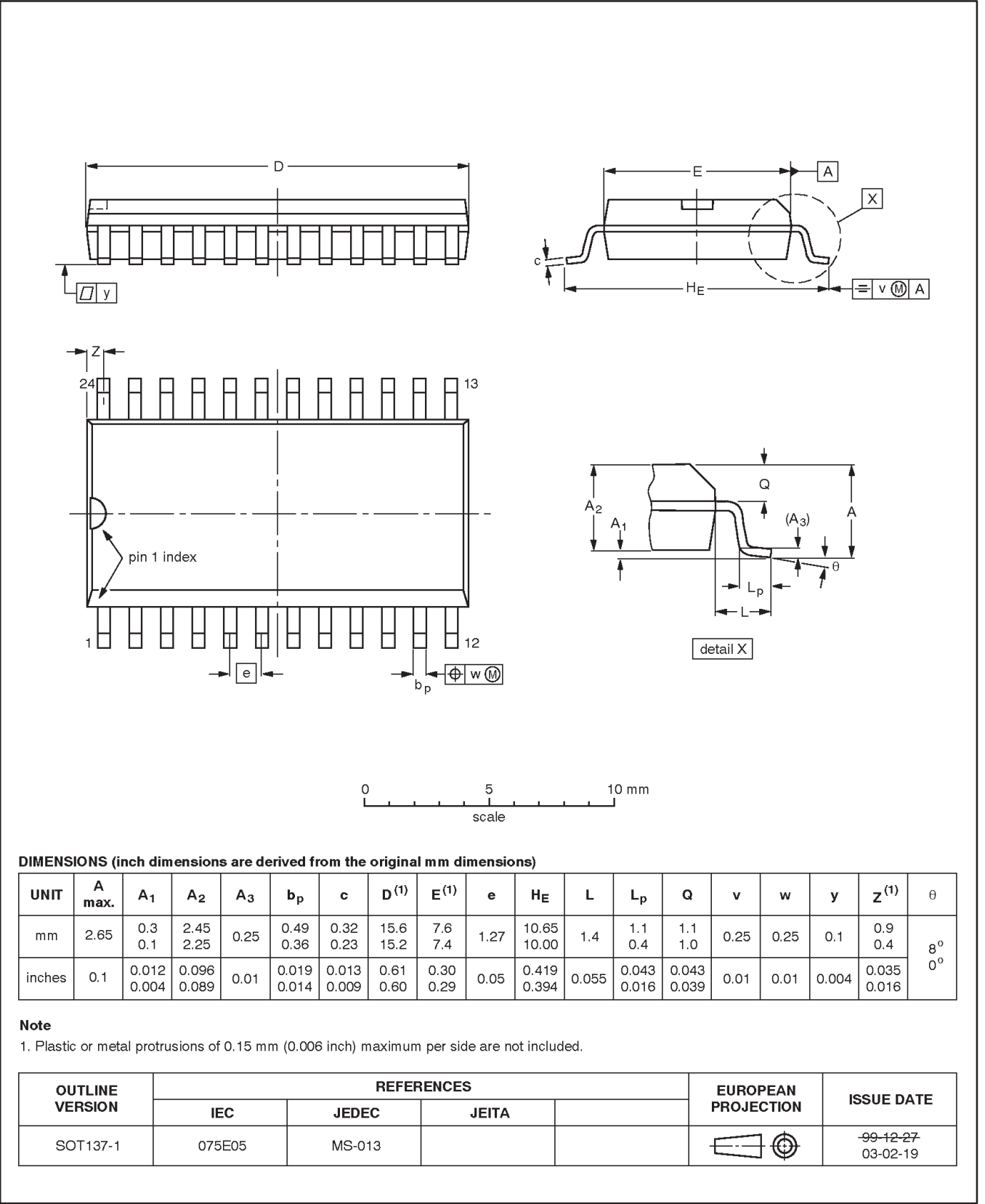


10-bit bus interface latches, non-inverting/inverting
(3-State)

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SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1



10-bit bus interface latches, non-inverting/inverting (3-State)

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REVISION HISTORY

Rev	Date	Description
_4	20040123	Product data (9397 750 12746). ECN 853-1208 A15379 of 22 January 2004. Replaces Product specification 74F841/842/843/845/846_3 dated 1999 Jun 23 (9397 750 06143). Modifications: <ul style="list-style-type: none"> Delete all references to 74F843, 74F845, 74F846 (products discontinued).
_3	19990623	Product specification (9397 750 06143). ECN 853-1208 21851 of 23 June 1999. Replaces datasheet 74F841/842/843/844/845/846 of 1999 Jan 08.

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